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EXAMINER	
MILORD, MARCEAU	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/699,019	Applicant(s) ROFOUGARAN, AHMADREZA	
	Examiner Marceau Milord	Art Unit 2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *27 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claim 27 is objected to because of the following informalities: the word "te", on page 90, line 20 in claim 27, should be written "the". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-19, 31-53, are rejected under 35 U.S.C. 103(a) as being unpatentable over Stikvoort (US Patent No 6236847 B1) in view of Hornak et al (US Patent No 5974306).

Regarding claims 1-3, Stilvoort discloses a notch filter (fig. 1), comprising: a first polyphase filter (16 of fig. 1) to output a plurality of phases (col. 3, lines 6-32); and a second polyphase filter (19 of fig. 1) having an input to receive the first phase and an input to receive the first phase (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

However, Stilvoort does not specifically disclose the feature of an inverted first phase having an input to receive the inverted first phase and an inverted input to receive the first phase.

On the other hand, Hornak et al, from the same field of endeavor, discloses an image-rejecting receiver comprises a tunable mixer stage, a time-share I-Q mixer stage, a complex

mixer, and an image rejecter. The time-share IQ mixer stage includes a switch assembly, in phase and quadrature polarity inverters, and a clock generator. The switch assembly generates pulses and distributes them in alternation to the polarity inverters (col. 4, lines 14-65; col. 5, lines 1-38). Furthermore, the distribution switch distributes both in phase and inverse-phase pulses along the in phase path, and distributes both quadrature and inverse-quadrature pulses along the quadrature path. Thus, polarity inverters are required along the in phase and quadrature paths to yield the desired in phase and quadrature components (col. 6, lines 15-61; col. 7, line 6- col. 8, line 43; col. 10, lines 35-57; col. 11, lines 20-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Hornak to the system of Stilvoort in order to provide an integrated circuit receiver with polarity inverter that can be inserted at either the signal input, or the output of the first stage mixer.

Regarding claim 4, Stilvoort as modified discloses a notch filter (fig. 1), wherein the first polyphase filter (16 of fig. 1) comprises a plurality of resistors and capacitors arranged in a polyphase structure to generate a zero at a particular frequency, the first polyphase filter outputting the quadrature signal when the input signal has a frequency at the particular frequency (fig. 4; col 5, lines 15-65).

Regarding claims 5-7, Stilvoort as modified discloses a notch filter (fig. 1), wherein the second polyphase filter (19 of fig. 1) comprises a plurality of resistors and capacitors arranged in a second polyphase structure to reject the quadrature signal at the particular frequency (fig. 6; col. 5, line 59- col. 7, line 14).

Regarding claim 8, Stilvoort as modified discloses a notch filter (fig. 1), wherein the first polyphase filter (16 of fig. 1) comprises first, second, third and fourth inputs adapted to receive

the input signal, the input signal being differential, the first and fourth inputs being coupled together to receive a first one of the differential input signals and the second and third inputs being coupled together to receive a second one of the differential input signals fig. 4; col 5, lines 15-65).

Regarding claim 9, Stilvoort as modified discloses a notch filter (fig. 1), wherein the first polyphase filter (16 of fig. 1) further comprises a first resistor having a first end coupled to the first input, a first capacitor having a first end coupled to the first input, a second capacitor having a first end coupled to the second input and a second end coupled to a second end of the first resistor to form a first output, a second resistor having a first end coupled to the second input, a third capacitor having a first end coupled to the third input and a second end coupled to a second end of the second resistor to form a second output, a third resistor having a first end coupled to the third input, a fourth capacitor having a first end coupled to the fourth input and a second end coupled to a second end of the third resistor to form a third output, and a fourth resistor having a first end coupled to the fourth input and a second end coupled to a second end of the first capacitor to form a fourth output (figs. 5-6; col. 5, line 59- col. 7, line 14).

Claim 10 contain similar limitations addressed in claim 1, and therefore is rejected under a similar rationale.

Regarding claim 11, Stilvoort as modified discloses a notch filter (fig. 1), wherein the second polyphase filter (19 of fig. 1) comprises fifth, sixth, seventh and eighth inputs, a fifth resistor having a first end coupled to the fifth input, a fifth capacitor having a first end coupled to the fifth input, a sixth capacitor having a first end coupled to the sixth input and a second end coupled to a second end of the fifth resistor, a sixth resistor having a first end

coupled to the sixth input, a seventh capacitor having a first end coupled to the seventh input and a second end coupled to a second end of the sixth resistor, a seventh resistor having a first end coupled to the seventh input, a eighth capacitor having a first end coupled to the eighth input and a second end coupled to a second end of the seventh resistor to form a seventh output, and a eighth resistor having a first end coupled to the eighth input and a second end coupled to a second end of the first capacitor to form a eighth output, and wherein the second output of the first polyphase filter is coupled to the eighth input of the second polyphase filter and the fourth output of the first polyphase filter is coupled to the sixth input of the second polyphase filter (figs. 5-6; col. 5, line 59- col. 7, line 14).

Regarding claims 12-16, Stilvoort discloses a notch filter (fig. 1), comprising: a first polyphase filter (16 of fig. 1) including an input, and an output having a non-inverted output (col. 3, lines 6-32); and a second polyphase filter (19 of fig. 1) having an input comprising a non-inverted, the non-inverted output of the first polyphase filter (16 of fig. 1) being coupled to the input of the second polyphase filter (19 of fig. 1) and the output of the first polyphase filter being coupled to the non inverted input of the second polyphase filter (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

However, Stilvoort does not specifically disclose the feature of an inverted output having an inverted input being coupled to the non-inverted input.

On the other hand, Hornak et al, from the same field of endeavor, discloses an image-rejecting receiver comprises a tunable mixer stage, a time-share I-Q mixer stage, a complex mixer, and an image rejecter. The time-share IQ mixer stage includes a switch assembly, in phase and quadrature polarity inverters, and a clock generator. The switch assembly generates

pulses and distributes them in alternation to the polarity inverters (col. 4, lines 14-65; col. 5, lines 1-38). Furthermore, the distribution switch distributes both in phase and inverse-phase pulses along the in phase path, and distributes both quadrature and inverse-quadrature pulses along the quadrature path. Thus, polarity inverters are required along the in phase and quadrature paths to yield the desired in phase and quadrature components (col. 6, lines 15-61; col. 7, line 6- col. 8, line 43; col. 10, lines 35-57; col. 11, lines 20-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Hornak to the system of Stilvoort in order to provide an integrated circuit receiver with polarity inverter that can be inserted at either the signal input, or the output of the first stage mixer.

Regarding claim 17, Stilvoort as modified discloses a notch filter (fig. 1), wherein the input to the first polyphase filter (16 of fig. 1) comprises first, second, third and fourth inputs, the first and fourth inputs being coupled together to receive the first one of the differential signals and the second and third inputs being coupled together to receive the second one of the differential input signals (fig. 4; col 5, lines 15-65).

Regarding claim 18, Stilvoort as modified discloses a notch filter (fig. 1), wherein the output of the first polyphase filter (16 of fig. 1) comprises first, second, third and fourth outputs, the first polyphase filter further comprising a first resistor having a first end coupled to the first input, a first capacitor having a first end coupled to the first input, a second capacitor having a first end coupled to the second input and a second end coupled to a second end of the first resistor to form the first output, a second resistor having a first end coupled to the second input, a third capacitor having a first end coupled to the third input and a second end coupled to a second end of the second resistor to .form the second output, a third resistor having a first end coupled to

the third input, a fourth capacitor having a first end coupled to the fourth input and a second end coupled to a second end of the third resistor to form the third output, and a fourth resistor having a first end coupled to the fourth input and a second end coupled to a second end of the first capacitor to form the fourth output, the non-inverted output of the first polyphase filter comprising the second output and the inverted output of the first polyphase circuit comprising the fourth output (figs. 5-6; col. 5, line 59- col. 7, line 14).

Regarding claim 19, Stilvoort as modified discloses a notch filter (fig. 1), wherein the input of the second polyphase filter (19 of fig. 1) comprises fifth, sixth, seventh and eighth inputs, the second polyphase filter further comprising a fifth resistor having a first end coupled to the fifth input, a fifth capacitor having a first end coupled to the fifth input, a sixth capacitor having a first end coupled to the sixth input and a second end coupled to a second end of the fifth resistor, a sixth resistor having a first end coupled to the sixth input, a seventh capacitor having a first end coupled to the seventh input and a second end coupled to a second end of the sixth resistor, a seventh resistor having a first end coupled to the seventh input, a eighth capacitor having a first end coupled to the eighth input and a second end coupled to a second end of the seventh resistor to form a seventh output, and a eighth resistor having a first end coupled to the eighth input and a second end coupled to a second end of the first capacitor to form a eighth output, the sixth input comprising the non-inverted input to the second polyphase filter and the eighth input comprising the inverted input to the second polyphase circuit (figs. 5-6; col. 5, line 59- col. 7, line 14).

Regarding claims 31-33, 36-40, 44-45, Stilvoort discloses a circuit (fig. 1), comprising: a mixer 94 of fig. 1) having an output including a mixed signal output and an inverted mixed

signal output (col. 3, lines 6-32); and a polyphase filter (16 of fig. 1) having an input including a non-inverted input coupled to the inverted mixed signal output, and an inverted input coupled to the non-inverted mixed signal output (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

However, Stilvoort does not specifically disclose the feature of an inverted output having an inverted input being coupled to the non-inverted input.

On the other hand, Hornak et al, from the same field of endeavor, discloses an image-rejecting receiver comprises a tunable mixer stage, a time-share I-Q mixer stage, a complex mixer, and an image rejecter. The time-share IQ mixer stage includes a switch assembly, in phase and quadrature polarity inverters, and a clock generator. The switch assembly generates pulses and distributes them in alternation to the polarity inverters (col. 4, lines 14-65; col. 5, lines 1-38). Furthermore, the distribution switch distributes both in phase and inverse-phase pulses along the in phase path, and distributes both quadrature and inverse-quadrature pulses along the quadrature path. Thus, polarity inverters are required along the in phase and quadrature paths to yield the desired in phase and quadrature components (col. 6, lines 15-61; col. 7, line 6- col. 8, line 43; col. 10, lines 35-57; col. 11, lines 20-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Hornak to the system of Stilvoort in order to provide an integrated circuit receiver with polarity inverter that can be inserted at either the signal input, or the output of the first stage mixer.

Regarding claim 34, Stilvoort as modified discloses a circuit (fig. 1), wherein the polyphase filter comprises an output having a notch at a particular frequency (fig. 4; col 5, lines 15-65).

Regarding claim 35, Stilvoort as modified discloses a circuit (fig. 1), wherein the polyphase filter comprises a plurality of resistors and capacitors arranged in a polyphase structure to generate a zero at the particular frequency (16 and 19 of fig. 1; col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 41, Stilvoort as modified discloses a circuit (fig. 1), wherein the polyphase filter comprises a plurality of resistors and capacitors arranged in a polyphase structure to generate a zero at a first frequency, and the second polyphase filter comprises a plurality of second resistor and capacitors arranged in a second polyphase structure to generate a zero at a second frequency different from the first frequency (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 42, Stilvoort as modified discloses a circuit (fig. 1), wherein the output of the polyphase filter (16 of fig. 1) comprises a notch at the first frequency, and the second polyphase filter (19 of fig. 1) comprises an output having a first notch at the first frequency and a second notch at the second frequency (col. 3, line 14- col. 4, line 31).

Regarding claim 43, Stilvoort as modified discloses a circuit (fig. 1), comprising a third filter having an input coupled to the output of the second polyphase filter, the third filter attenuating frequencies above a third frequency higher than the first and second frequencies (col. 3, line 40- col. 4, line 54).

Regarding claims 46-48, 52-53, Stilvoort discloses a circuit (fig. 1), comprising: a first polyphase filter (16 of fig. 1) having an output including a non-inverted output (col. 3, lines 6-32); and a second polyphase (19 of fig. 1) having an input including a non-inverted input coupled

to the output of the first polyphase (16 of fig. 1) and an input coupled to the non-inverted output of the first polyphase filter (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

However, Stilvoort does not specifically disclose the feature of an inverted input coupled to the non-inverted output; and an inverted in-phase component.

On the other hand, Hornak et al, from the same field of endeavor, discloses an image-rejecting receiver comprises a tunable mixer stage, a time-share I-Q mixer stage, a complex mixer, and an image rejecter. The time-share IQ mixer stage includes a switch assembly, in phase and quadrature polarity inverters, and a clock generator. The switch assembly generates pulses and distributes them in alternation to the polarity inverters (col. 4, lines 14-65; col. 5, lines 1-38). Furthermore, the distribution switch distributes both in phase and inverse-phase pulses along the in phase path, and distributes both quadrature and inverse-quadrature pulses along the quadrature path. Thus, polarity inverters are required along the in phase and quadrature paths to yield the desired in phase and quadrature components (col. 6, lines 15-61; col. 7, line 6- col. 8, line 43; col. 10, lines 35-57; col. 11, lines 20-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Hornak to the system of Stilvoort in order to provide an integrated circuit receiver with polarity inverter that can be inserted at either the signal input, or the output of the first stage mixer

Regarding claim 49, Stilvoort as modified discloses a circuit (fig. 1), wherein the first polyphase filter (16 of fig. 1) comprises a plurality of first resistors and capacitors arranged in a polyphase structure to generate a zero at a first frequency, and the second polyphase filter comprises a plurality of second resistor and capacitors arranged in a second polyphase structure

to generate a zero at a second frequency different from the first frequency (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 50, Stilvoort as modified discloses a circuit (fig. 1), wherein the output of the first polyphase filter (16 of fig. 1) comprises a notch at the first frequency, and the second polyphase filter (19 of fig. 1) comprises an output having a first notch at the first frequency and a second notch at the second frequency (col. 3, line 14- col. 4, line 31).

Regarding claim 51, Stilvoort as modified discloses a circuit (fig. 1), comprising a third filter having an input coupled to the output of the second polyphase filter, the third filter attenuating frequencies above a third frequency, the third frequency being higher than the first and second frequencies (col. 3, line 40- col. 4, line 54).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 20-30, 54-66 are rejected under 35 U.S.C. 102(e) as being anticipated by Stikvoort (US Patent No 6236847 B1).

Regarding claim 20, Stikvoort discloses a notch filter (fig. 1), comprising: generating means (16 of fig. 1) for generating an output signal comprising a plurality of phases of an input signal (col. 3, lines 6-32); and notching means (19 of fig. 1) for notching a particular frequency of the input signal as a function of the phases (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 21, Stikvoort discloses a notch filter (fig. 1), wherein the input signal comprises a differential signal (col. 3, lines 6-32).

Regarding claim 22, Stikvoort discloses a notch filter (fig. 1), wherein the generating means (16 of fig. 1) further comprises means for generating the output signal with quadrature outputs when the input signal includes the particular frequency (col. 4, lines 1-49).

Regarding claim 23, Stikvoort discloses a notch filter (fig. 1), wherein the notching means comprising means for rejecting the quadrature signal at the particular frequency (col. 2, lines 19-52; col 3, lines 14-46).

Regarding claim 24, Stikvoort discloses a notch filter (fig. 1), wherein the particular frequency is an odd harmonic of the input signal (col. 3, line 34- col. 4, line 17).

Regarding claim 25, Stikvoort discloses a notch filter (fig. 1), wherein the particular frequency is a third harmonic of the input signal (col. 1, line 61- col. 2, line 21; col. 3, line 34- col. 4, line17).

Regarding claim 26, Stikvoort discloses a method of notching a particular frequency of a signal (fig. 1), comprising: generating (16 of fig. 1) an output signal comprising a plurality of phases of an input signal (col. 3, lines 6-32); and notching the particular frequency of the input signal as a function of the phases (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 27, Stikvoort discloses a method of notching a particular frequency of a signal (fig. 1), wherein the generation of the output signal comprises generating the output signal with quadrature outputs when the input signal includes the particular frequency (col. 4, lines 1-49).

Regarding claim 28, Stikvoort discloses a method of notching a particular frequency of a signal (fig. 1), wherein the notching of the particular frequency comprises rejecting the quadrature signal at the particular frequency (col. 2, lines 19-52; col 3, lines 14-46).

Regarding claim 29, Stikvoort discloses a method of notching a particular frequency of a signal (fig. 1), wherein the particular frequency is an odd harmonic of the input signal (col. 3, line 34- col. 4, line 17).

Regarding claim 30, Stikvoort discloses a method of notching a particular frequency of a signal (fig. 1), wherein the particular frequency is a third harmonic of the input signal (col. 1, line 61- col. 2, line 21; col. 3, line 34- col. 4, line17).

Regarding claim 54, Stikvoort discloses a circuit (fig. 1) comprising: mixing means (4 of fig. 1) for mixing two signals and outputting a mixed signal and an inverted mixed signal (col. 3, lines 6-56); and filtering means (14 of fig. 1) for notching a particular frequency of the mixed signal using a polyphase structure (16 and 19 of fig. 1; col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 55, Stikvoort discloses a circuit (fig. 1) wherein the polyphase structure comprises means for generating a zero at the particular frequency (16 and 19 of fig. 1; col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 56, Stikvoort discloses a circuit (fig. 1) further comprising a second filtering means (14 of fig. 1) for notching a second frequency of the mixed signal using a second polyphase structure (19 of fig. 1), the second frequency being different from the first frequency (col. 4, lines 1-49).

Regarding claim 57, Stikvoort discloses a circuit (fig. 1) wherein the polyphase structure (16 and 19 of fig. 1) comprises, means for generating a zero at the particular frequency, and the second polyphase structure comprises means for generating a second zero at the second frequency (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 58, Stikvoort discloses a circuit (fig. 1) further comprising a third filtering means for attenuating frequencies above a third frequency of the mixed signal, the third frequency being higher than the particular and second frequencies (col. 3, line 40- col. 4, line 54).

Regarding claim 59, Stikvoort discloses a circuit (fig. 1), comprising: first filtering means (14 of fig. 1) for notching a first frequency of a signal using a first polyphase structure (16 of fig. 1) and second filtering means for notching a second frequency of the signal using a second polyphase structure (19 of fig. 1), the second frequency being different from the first frequency (col. 3, lines 7- 56; col. 4, lines 32-54).

Regarding claim 60, Stikvoort discloses a circuit (fig. 1), wherein the first polyphase structure comprises means for generating a first zero at the first frequency, and the second polyphase structure comprises means for generating a second zero at the second frequency (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 61, Stikvoort discloses a circuit (fig. 1), further comprising a third filtering means for attenuating frequencies above a third frequency of the signal, the third frequency being higher than the second frequency (col. 3, line 40- col. 4, line 54).

Regarding claim 62, Stikvoort discloses a method of filtering a signal (fig. 1) comprising notching a particular frequency of the signal using a polyphase structure (16 and 19 of fig. 1;col. 3, lines 6-51)

Regarding claim 63, Stikvoort discloses a method of filtering a signal (fig. 1) wherein the notching of the particular frequency comprises generating a zero at the particular frequency using the polyphase structure (col. 3, lines 14-51; col. 1, line 48- col. 2, line 29).

Regarding claim 64, Stikvoort discloses a method of filtering a signal (fig. 1) further comprising notching a second frequency of the signal using a second polyphase structure, the second frequency being different from the first frequency (col. 3, lines 7- 56; col. 4, lines 32-54).

Regarding claim 65, Stikvoort discloses a method of filtering a signal (fig. 1) wherein the notching of the particular frequency comprises generating a zero at the particular frequency using the polyphase structure, and the notching of the second frequency comprises generating a second zero at the second frequency using the second polyphase structure (col. 3, line 33- col. 4, line 31; col. 1, line 48- col. 2, line 29).

Regarding claim 66, Stikvoort discloses a method of filtering a signal (fig. 1) further comprising attenuating frequencies above a third frequency of the mixed signal, the third frequency being higher than the particular and second frequencies (col. 1, line 61- col. 2, line 21; col. 3, line 34- col. 4, line17).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yu-Hong US Patent No 6118984 discloses a dual conversion radio frequency transceiver.

Arevato US Patent No 6147576 discloses a method for designing filters.

Narumi et al US Patent No 6118811 discloses a transceiver which has a digital signal processor that can insert calibration signals of known levels and frequency into transmitters for calibration and correction of transmitter parameters.

Brehmer et al US Patent No 5283484 discloses a voltage limiter, which includes a resistor receiving an input signal on a first terminal and providing an output signal on a second terminal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 703-306-3023. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian C. Chin can be reached on 703-308-6739. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

MARCEAU MILORD

Marceau Milord
Examiner
Art Unit 2682